	Date	Version No.	1.0
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PRODUCT NAME : DRLNA-A MODULE

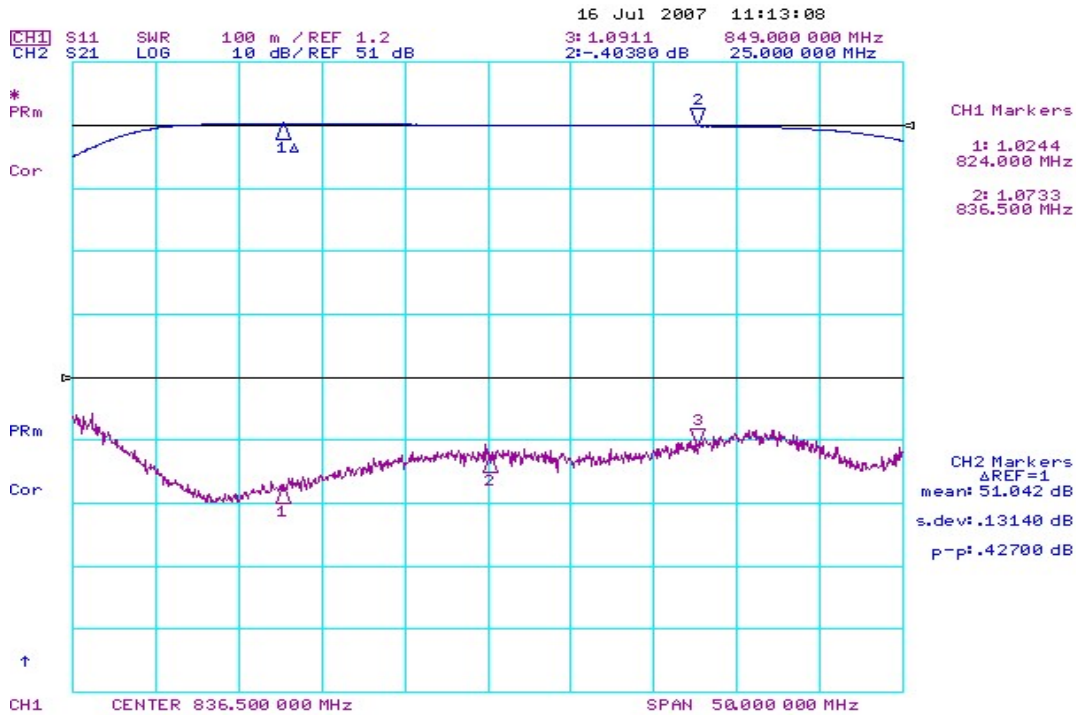
Part NO : DRLNA-A

품 목		규 격	특기사항	
Frequency Range		2G:824~849MHz, 3G:1940~1960MHz	2G,3G : Rx	
2G	GAIN	51dB ± 0.3dB이내	(ATT0dB설정)	
	GAIN Flatness	0.5dBp-p 이하		
	IN/OUT VSWR	1.2 : 1 이하		
	IMD	68dBc 이상	출력기준 0dBm/1tone	
	Noise Figure	1.5dB 이하	온도포함	
	Output Detector Range	출력기준 : 15dBm@3.5V±0.05Vdc	15dBm~-20dBm(CW기준) (dB당 최소 30mv 이상 가변)	
	ATT Range / ATT Control Error	0 ~ 15dB(± 0.5dB이내)	(Step Size: 0.5dB)	
	SG Level	출력기준 : MarkerΔ± 0.3dBm이내	823.64MHz(-61dBm입력)	
	Multi path 이득	5dB (±0.30이내)		
	Output Monitor	20dB (±0.50이내)	JIG 확인	
3G	GAIN	51.5dB ± 0.3dB이내	(ATT0dB설정)	
	GAIN Flatness	0.5dBp-p 이하		
	IN/OUT VSWR	1.2 : 1 이하		
	IMD	68dBc 이상	출력기준 0dBm/1tone	
	Noise Figure	1.5dB 이하	온도포함	
	Output Detector Range	출력기준 : 15dBm@3.5V±0.05Vdc	15dBm~-20dBm(CW기준) (dB당 최소 30mv 이상 가변)	
	SG Level	출력기준 : MarkerΔ± 0.3dBm이내	1945.3MHz(-61.5dBm입력)	
	Multi path 이득	5dB (±0.30이내)		
	ATT Range / ATT Control Error	0 ~ 15dB(± 0.5dB이내)	(Step Size: 0.5dB)	
	Output Monitor	20dB (±0.50이내)	JIG 확인	
공통	AMP ALARM	Normal : 1 Alarm : 0	JIG LED확인	
	DC Supply Voltage	+9 V, +6.5V		
	Consumption Current	+9v	200mA 이하	
		+6.5v	1000mA 이하	
	치수 검사(치수 및 재질)	승인원 기준		
	외관 검사(SILK 및 도장,도금)	승인원 기준		
조립 검사(조립상태)	승인원 기준			

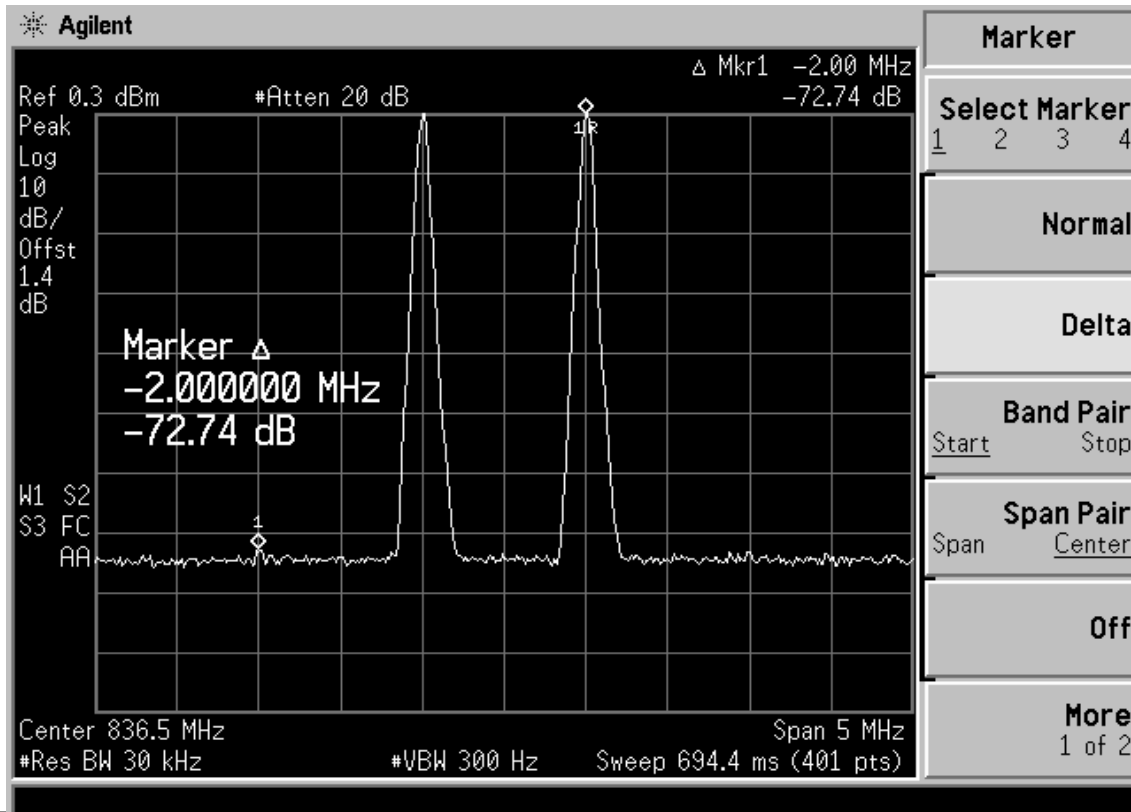
Graph.

▷ 2G

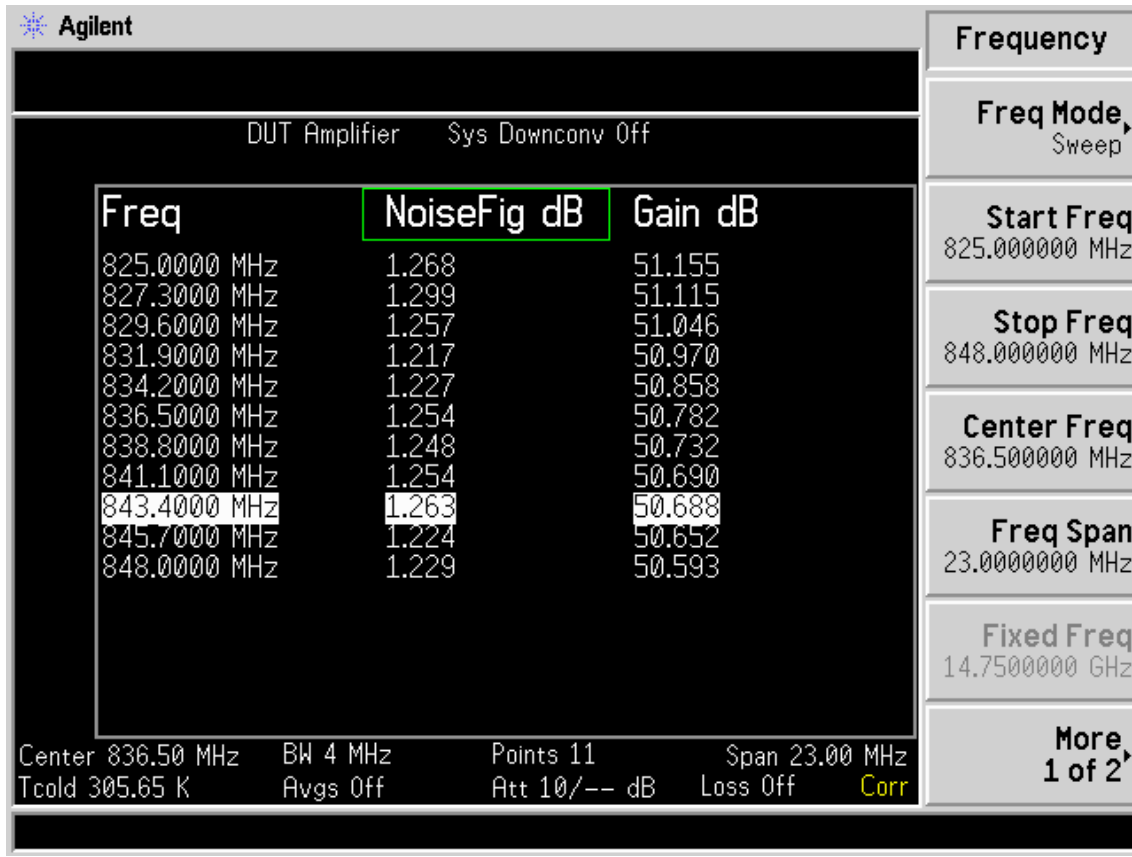
GAIN, Ripple, VSWR



IMD

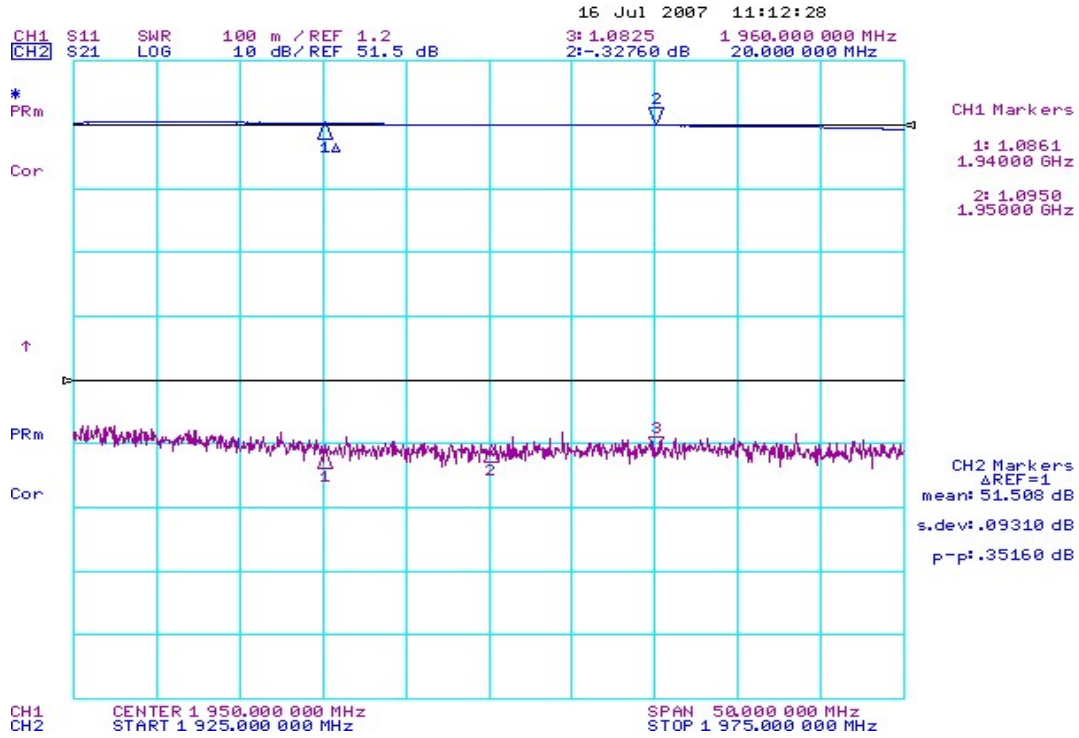


Noise Figure

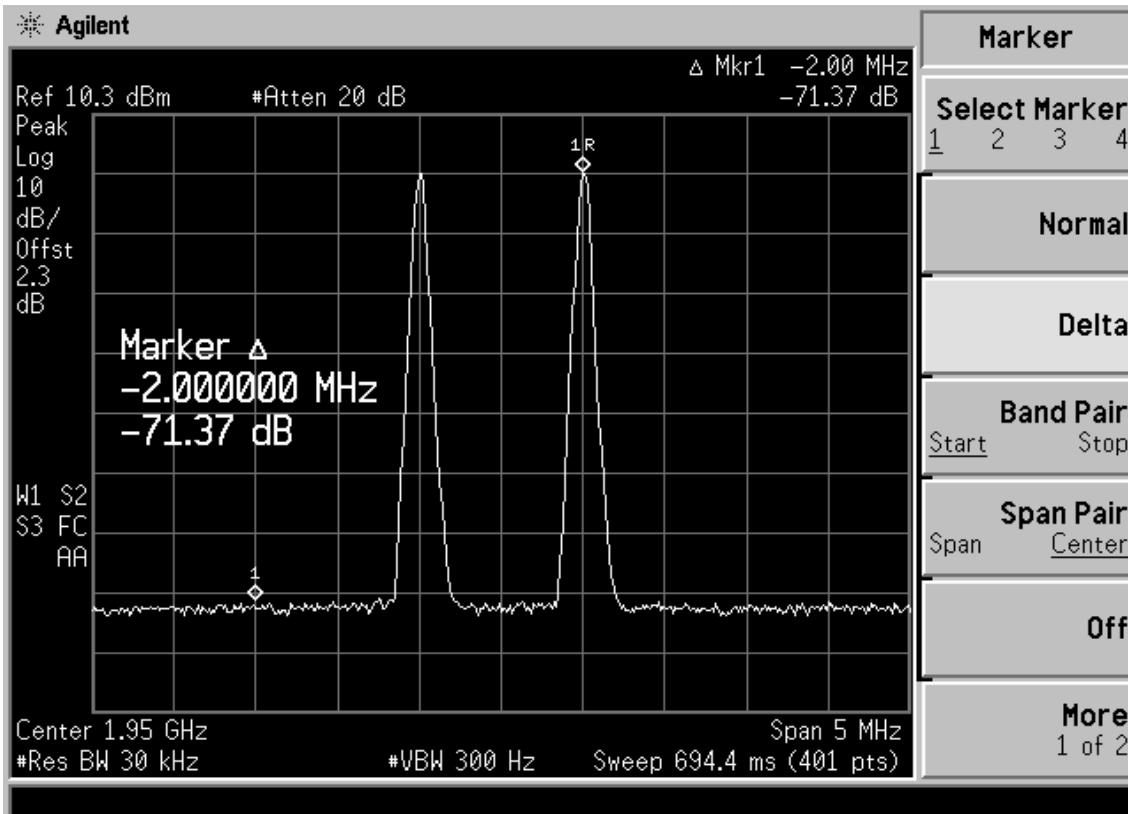


▷ 3G

GAIN, Ripple, VSWR



IMD



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Noise Figure

